Hardware Design of Advanced Motor Drive Controller (AMDC)

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Contents

1 Introduction

This document describes the Advanced Motor Drive Controller (AMDC) hardware and the decisions that were made to arrive at the specific components used. There are multiple systems of AMDC that must work together to allow user tasks to easily control power electronics. Each system is outlined throughout this document.

The control hardware consists of two physical printed circuit boards (PCBs), connected via high pin count connectors. The System on Module (SOM) PCB plugs into connectors on the I/O Carrier PCB.

2 Quick Start User Guide

AMDC has numerous interfaces and jumpers which must be configured correctly to enable operation.

2.1 Rear-Mounted Screw Terminal Blocks

- VIN should be provided 24V
- VDRIVE should be provided 15V
- ESTOP needs to be shorted to enable digital drive output PWM signals

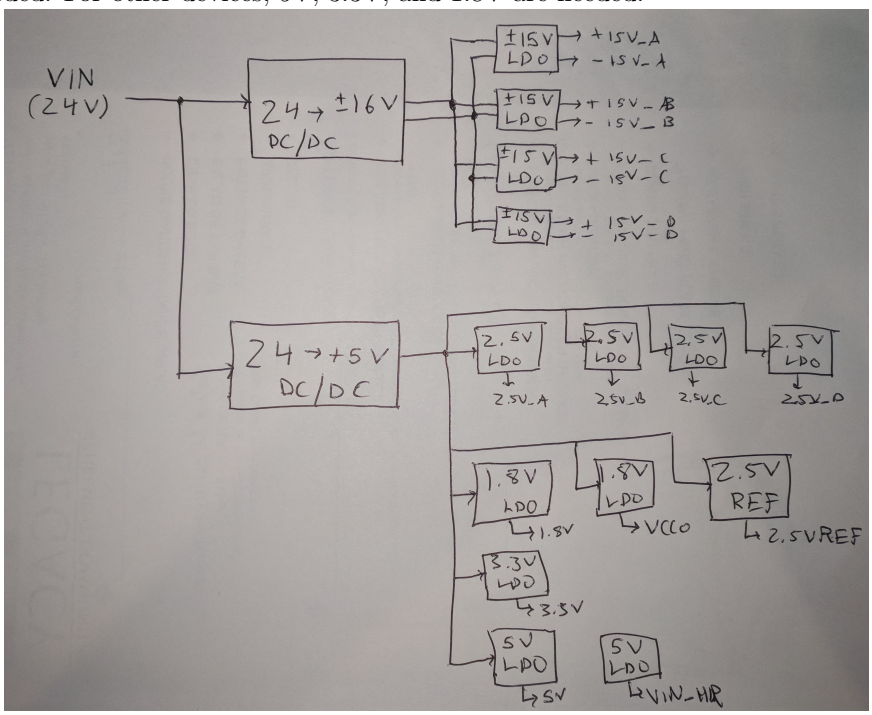
2.2 Jumpers

- JP11 / JP12 select modes for USB OTG
  - Short JP12 for USB Host Mode
  - Short JP11 on lower side for Host/Device Mode
  - Short JP11 on top side for OTG Mode
- JP9 enables JTAG reset via 2x7 pin header; not needed for JTAG-SMT2 usage
- Short JP1 to provide 5V supply to encoder connection
- GPIO configuration (see silkscreen on PCB)
  - JP3 / JP5 select GPIO voltage levels for bank A / B.
  - JP2 / JP4 select GPIO direction for bank A / B.
- JP8 / JP9 select drive output signal translation voltage levels
- JP6 / JP7 select drive output supply voltage levels
- **JP10 selects CTRL signal for DC/DC switching power converters**
- **JP13 / JP14 / JP15 are needed to enable DC/DC power converter outputs**

3 Power Supplies / Regulators

AMDC requires several different voltages throughout the board for a variety of different usages. All power is brought onto AMDC via one 24V input (and one voltage supply for gate drivers). Two switching DC/DC modules are used to convert the 24V input to ±16V and +5.5V.

Next, multiple low-dropout (LDO) regulators are used to provide clean voltage supplies at a variety of levels. For the Analog Signal Measurement system, noise-free ±15V and 2.5V supplies are needed. For other devices, 5V, 3.3V, and 1.8V are needed.



4 Processor / Programmable Logic

To enable high speed power electronic control, capable processing power must be used.

4.1 PicoZed 7030

The PicoZed 7030 provides an easy-to-use System-on-Module (SoM) that meets all proposed goals:

- Dual core capable of running embedded Linux / controller software
- Floating Point Unit (FPU)
- Sufficient I/O for board interfaces

4.1.1 Relevant Acronyms

PS Processing System : main processor running control algorithm and Linux, etc

PL Programmable Logic : configurable hardware

MIO Multiplexed I/O : I/O shared for different modules

4.1.2 Technical Specifications

SoC XC7Z030-1SBG485

Memory 1 GB of DDR3 SDRAM, 128 Mb of QSPI Flash, 4 GB eMMC

Communications 10/100/1000 Ethernet PHY, USB 2.0 PHY, User I/O

I/O 148 User I/O (135 PL, 13 PS MIO), PL I/O configurable as up to 65 LVDS pairs or 135 single-ended I/O, 4 GTX Transceivers

Other JTAG configuration port accessible via I/O connectors, PS JTAG pins accessible via I/O connectors, 33.33 MHz oscillator

Software Linux BSP and reference design

4.1.3 Helpful Links

- PicoZed Technical Specifications
- PicoZed Carrier Design Guide
- PicoZed 7030 H/W Users Guide

5 Analog Signal Measurement

AMDC system provides an analog signal measurement system that allows users to use high precision analog values in control algorithms. This design is informed by previous control board designs with a goal of the following improvements:

- Isolated differential signal input, without common ground between cables
- Tuned active low-pass anti-aliasing filters on analog signal input
- Noise immune connectors for analog signal input (RJ45)

5.1 Analog Input Signal Path

AMDC PCB includes two analog front-end designs to test different approaches for signal conditioning path. The two different approaches result in pros and cons for each. Approach #1 (discrete in-amp architecture) implements the correct gain needed for AMDC, but has less common-mode rejection and is more susceptible to noise. Approach #2 (single device in-amp) uses laser-trimmed internal resistors to set gain, which results in much higher common-mode rejection, but has a set gain which is not ideal for AMDC.

5.1.1 Approach #1

Signals enter the ADC front end conditioning path at high voltage bipolar levels on both $V_{in}+$ and $V_{in}-$. These voltages are then scaled, subtracted, and offset by two stages of op amps. Finally, a voltage follower feeds the input into the ADC. See Figure 1 for schematic implementation. The given in-amp architecture is typically referred to as the *three op amp in-amp* [1] and follows this equation:

$$V_{out} = V_{in} \cdot \frac{R_3}{R_2}\left[1 + \frac{2R_1}{R_G}\right] + V_{offset}$$

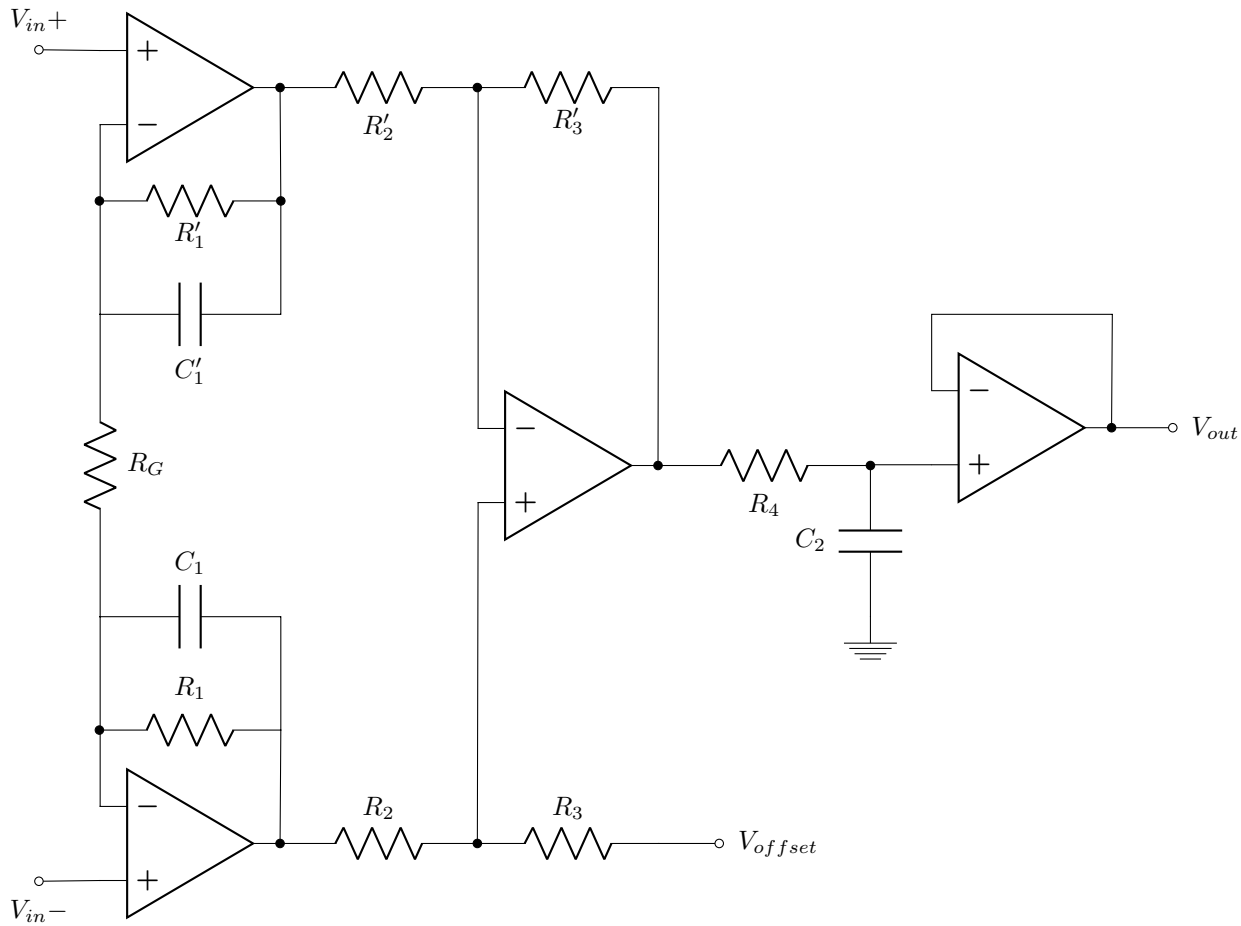


Figure 1: Analog Signal Path per Figure 1 of [1]

Setting $R_G = 2k\Omega, R_1 = R_1' = 1k\Omega, R_2 = R_2' = 16k\Omega, R_3 = R_3' = 1k\Omega, V_{offset} = 2.5V$, then the signal path correctly scales a -10V..10V input signal to a 0V..5V pseduo-differential signal centered at +2.5V to feed into the ADC:

$$V_{out} = \frac{1}{8}V_{in} + 2.5V$$

This architecture was chosen specifically for the AMDC project. The voltage sources being measured are not fixed at the time of controller board design; each input may come from a variety of sensors. Because of this, the AMDC board cannot assume anything with respect to common mode voltages, thus common mode rejection (CMR) must be high.

The CMR of the in-amp topology shown in Figure 1 depends upon the ratio matching of R_3/R_2 to R_3'/R_2'. Also, because of the symmetry of this configuration, common mode errors in the input amplifiers, if they track, tend to be canceled out by the subtractor output stage. These features explain the choice of this three op amp in-amp configuration — it is capable of delivering the highest performance.

5.1.2 Approach #2

This approach uses an IC that includes all op amps internally connected to form an in-amp. This means that resistor values can be trimmed to exact ratios, resulting in excellent CMR. Unfortunately, gains of < 1 are less common than ≥ 1, so there was a limited number of choices for devices. The INA2143 device was selected, with a fixed gain of 0.1x.

6 Digital Output

AMDC system provides numerous high-speed digital outputs for user control algorithms to utilize. These outputs are single-ended signals, swinging from 0V to a user-supplied voltage, V_{DRIVE}.

6.1 Digital Output Signal Path

1. 1.8V digital signal comes from PicoZed SoM module
2. Level shift to 5V
3. Use variable converter to level shift to V_{DRIVE}
4. Output via DB15 connector

6.2 Components

1. High-pin count connectors to SoM
   - Three 2x50 connectors
2. 13x ADG3308 (1.8V $\rightarrow$ 5V)
   - See part on DigiKey ($4.75 each / $62 total)
3. 15x TC4468 (5V $\rightarrow V_{DRIVE}$)
   - See part on DigiKey ($3.80 each / $57 total)
4. DB15 connectors
   - 6x DB15 high-density stacked "VGA"

7 Encoder Input

AMDC supports reading a standard rotary encoder to supply data to user control algorithms and to help test system. The encoder input is RS422 compliant (differential 5V signals).

7.1 Components

1. 1x MAX3097E Triple RS-422 Receiver
   - 3 channel RS422 receiver for $A, \bar{A}, B, \bar{B}, Z, \bar{Z}$
   - Alarm outputs for error in pulses
   - See part on DigiKey ($6.50 each / $6.50 total)

8 General Purpose I/O

24 general purpose input/outputs (GPIO) pins are available on AMDC at jumper-selected 3.3V or 5V levels. The user can also select GPIO direction via hardware jumpers as well as software configuration.

9 Multi-Board Interface

9.1 GTX transceiver based PCIe

Use GTX transceivers to implement four PCIe ports per AMDC. Enables a daisy chain connection between AMDC boards. Each PCIe port is x1, meaning there is one lane for each direction of communication. Using PCIe as the inter-board interface enables high data throughput between AMDCs.

In terms of hardware support for PCIe, it appears that the MGT* signals need to routed from the PicoZed SoM to PCIe connectors. An additional IC maybe needed to provide a reference clock. An IP core block is available from Xilinx to run on the PicoZed programmable logic to control this interface. See the page 9 of reference carrier card design [2] for implementation example.

NOTE: the multi-board interface was not included in the AMDC PCB preliminary design.

10 PCB Form Factor

AMDC PCB will reside in server rack box, having all connectors on one side of PCB for ease of access.

References

[1] A. Devices, "Basic three op amp in-amp configuration," Oct 2008. [Online]. Available: http://www.analog.com/media/en/training-seminars/tutorials/MT-063.pdf

[2] Avnet, "Picozed fmc carrier gen2," Mar 2016. [Online]. Available: http://zedboard.org/sites/default/files/documentations/PZCC_FMC_V2_Rev1_Schematic_160315.PDF